

-100V, -17A, 51mΩ P-channel Power SGT MOSFET

JMPL1050PU

Features

- Excellent $R_{DS(ON)}$ and Low Gate Charge
- 100% UIS Tested
- 100% ΔV_{ds} Tested
- Halogen-free; RoHS-compliant
- Pb-free plating

Applications

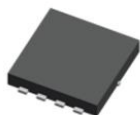
- Load Switch
- PWM Application
- Power Management

Product Summary

Parameters	Value	Unit
V_{DSS}	-100	V
$V_{GS(th)}_{Typ}$	-1.7	V
$I_D(@V_{GS}=-10V)$	-17	A
$R_{DS(ON)}_{Typ}(@V_{GS}=-10V)$	39	mΩ
$R_{DS(ON)}_{Typ}(@V_{GS}=-4.5V)$	51	mΩ



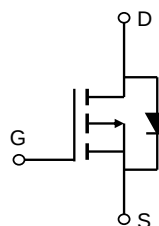
Top View



Bottom View



Pin Assignment



Schematic Diagram

PDFN3x3-8L

Ordering Information

Device	Marking	MSL	Form	Package	Reel(pcs)	Per Carton (pcs)
JMPL1050PU-13	PL1050P	1	Tape&Reel	PDFN3x3-8L	5000	50000

Absolute Maximum Ratings (@ $T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-to-Source Voltage	-100	V
V_{GS}	Gate-to-Source Voltage	± 20	V
I_D	Continuous Drain Current	$T_C = 25^\circ\text{C}$ $T_C = 100^\circ\text{C}$	A
I_{DM}	Pulsed Drain Current ⁽¹⁾	Refer to Fig.4	A
E_{AS}	Single Pulsed Avalanche Energy ⁽²⁾	165	mJ
P_D	Power Dissipation	$T_C = 25^\circ\text{C}$ $T_C = 100^\circ\text{C}$	W
T_J, T_{STG}	Junction & Storage Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Max	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient ⁽³⁾	48	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case	4.2	

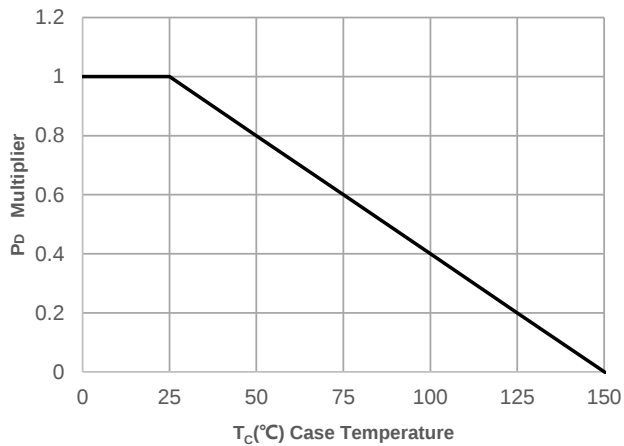
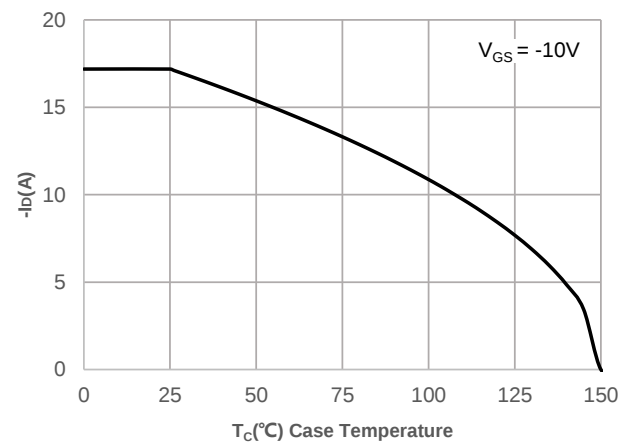
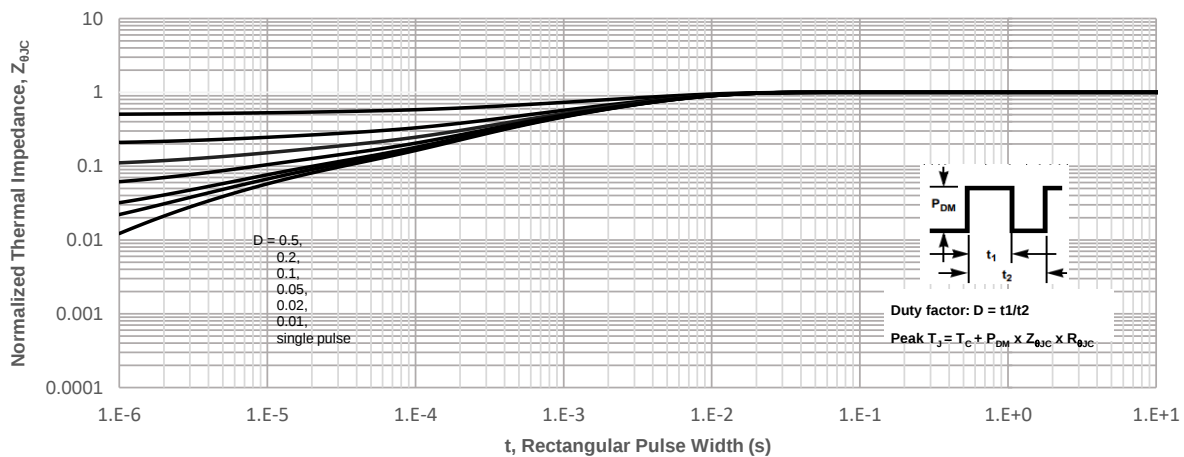
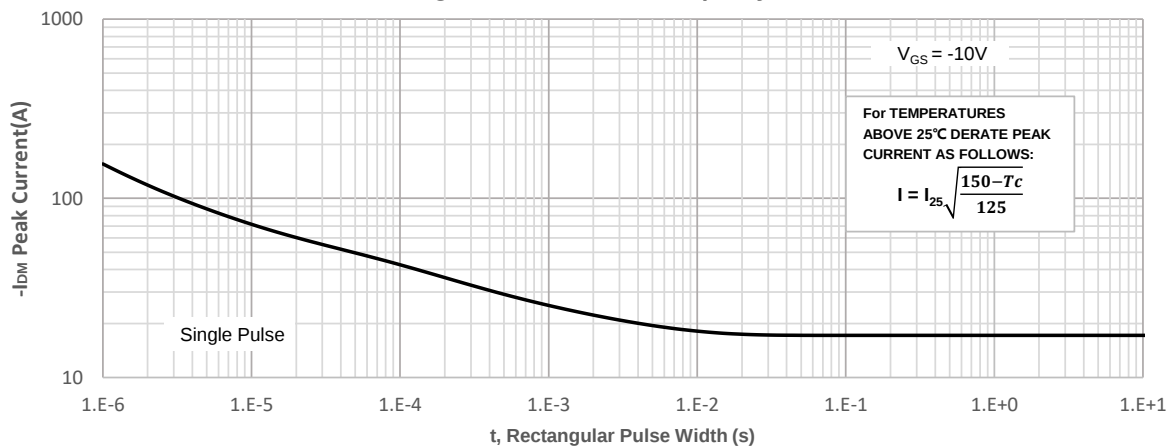
**Electrical Characteristics** ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	I _D = -250μA, V _{GS} = 0V	-100	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -80V, V _{GS} = 0V	-	-	-1.0	μA
I _{GSS}	Gate-Body Leakage Current	V _{DS} = 0V, V _{GS} = ±20V	-	-	±100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = -250μA	-1.2	-1.7	-2.2	V
R _{DS(ON)}	Static Drain-Source ON-Resistance ⁽⁴⁾	V _{GS} = -10V, I _D = -20A	-	39	51	mΩ
		V _{GS} = -4.5V, I _D = -15A	-	51	67	mΩ
Dynamic Characteristics						
R _g	Gate Resistance	f = 1MHz	-	7.5	-	Ω
C _{iss}	Input Capacitance	V _{GS} = 0V, V _{DS} = -50V, f = 1MHz	1261	1765	2383	pF
C _{oss}	Output Capacitance		147	205	277	pF
C _{rss}	Reverse Transfer Capacitance		12	17	24	pF
Q _g	Total Gate Charge	V _{GS} = 0 to -10V V _{DS} = -50V, I _D = -20A	19	27	36	nC
Q _{gs}	Gate Source Charge		-	7.4	-	nC
Q _{gd}	Gate Drain("Miller") Charge		-	4.1	-	nC
Switching Characteristics						
t _{d(on)}	Turn-On DelayTime	V _{GS} = -10V, V _{DD} = -50V I _D = -20A, R _{GEN} = 3Ω	-	7	-	ns
t _r	Turn-On Rise Time		-	6.5	-	ns
t _{d(off)}	Turn-Off DelayTime		-	38	-	ns
t _f	Turn-Off Fall Time		-	9.4	-	ns
Body Diode Characteristics						
I _S	Maximum Continuous Body Diode Forward Current		-	-	-17	A
I _{SM}	Maximum Pulsed Body Diode Forward Current		-	-	-69	A
V _{SD}	Body Diode Forward Voltage	V _{GS} = 0V, I _S = -20A	-		-1.2	V
trr	Body Diode Reverse Recovery Time	I _F = -20A, di/dt = 100A/us	35	49	67	ns
Qrr	Body Diode Reverse Recovery Charge		-	128	-	nC

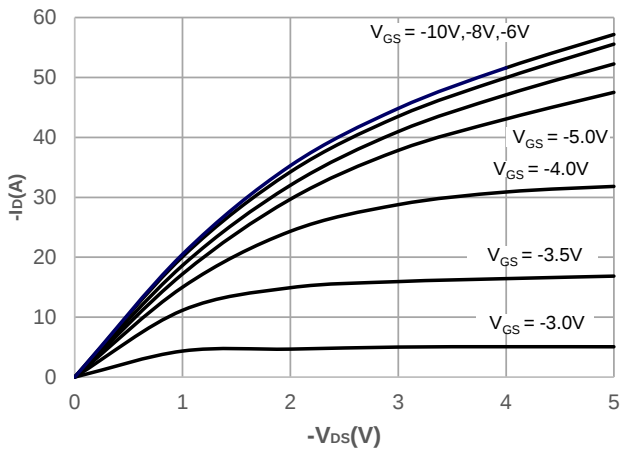
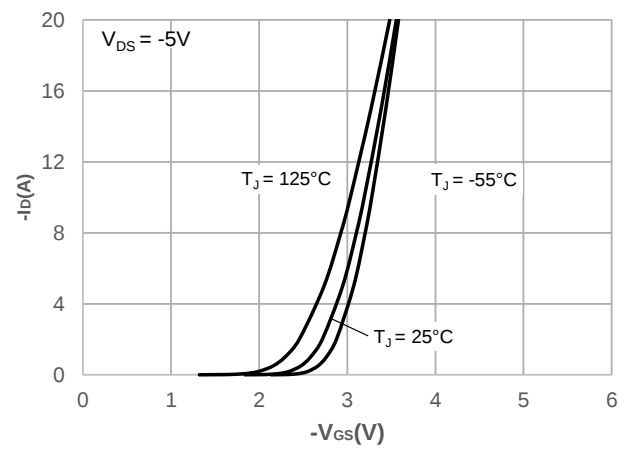
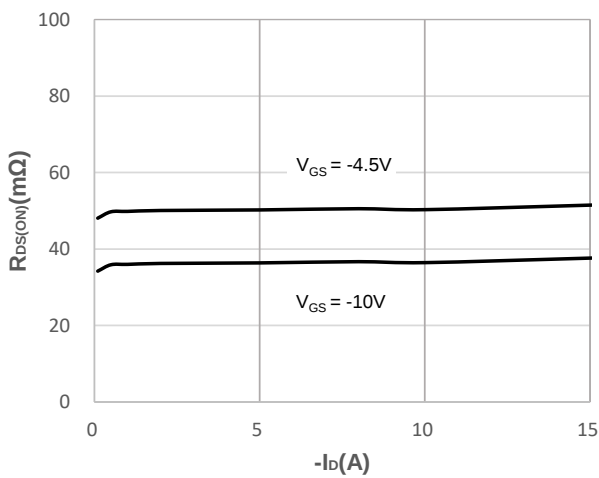
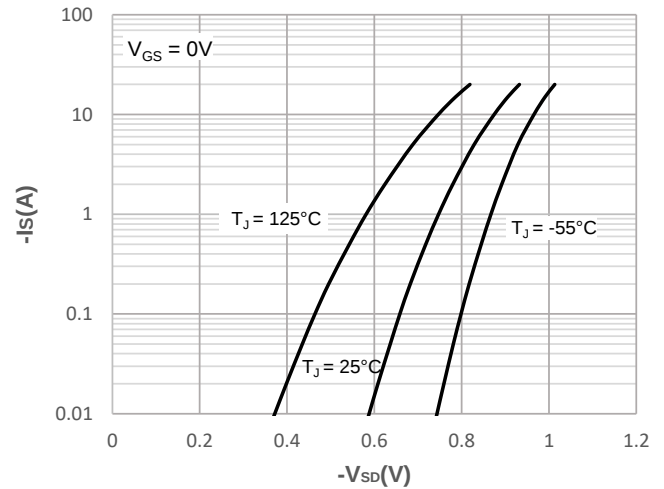
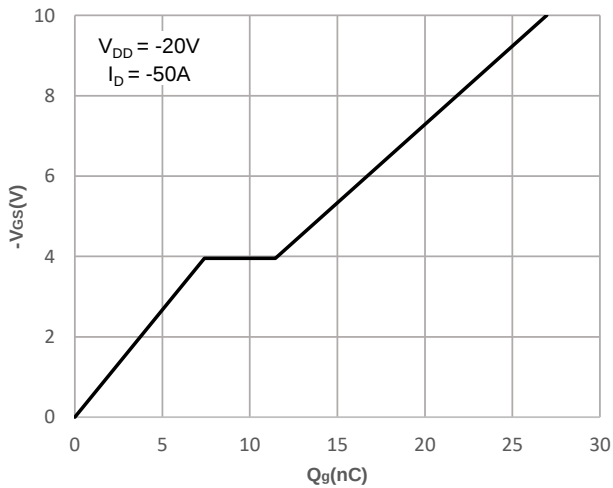
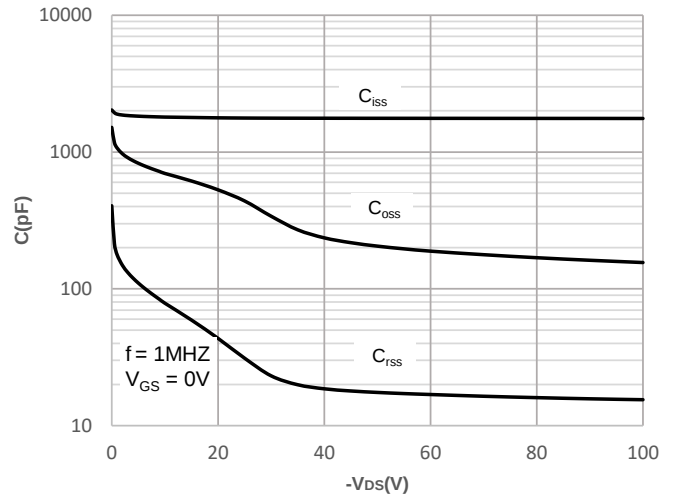
- Notes:
1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
 2. E_{AS} condition: Starting $T_J = 25^\circ\text{C}$, $V_{DD} = -50\text{V}$, $V_{GS} = -10\text{V}$, $R_G = 25\Omega$, $L = 3\text{mH}$, $I_{AS} = -10.5\text{A}$, $V_{DD} = 0\text{V}$ during time in avalanche.
 3. $R_{\theta JA}$ is measured with the device mounted on a 1inch^2 pad of 2oz copper FR4 PCB.
 4. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$.



Typical Performance Characteristics

Figure 1: Power De-rating

Figure 2: Current De-rating

Figure 3: Normalized Maximum Transient Thermal Impedance

Figure 4: Peak Current Capacity


Typical Performance Characteristics

Figure 5: Output Characteristics

Figure 6: Typical Transfer Characteristics

Figure 7: On-resistance vs. Drain Current

Figure 8: Body Diode Characteristics

Figure 9: Gate Charge Characteristics

Figure 10: Capacitance Characteristics


Typical Performance Characteristics

Figure 11: Normalized Breakdown voltage vs. Junction Temperature

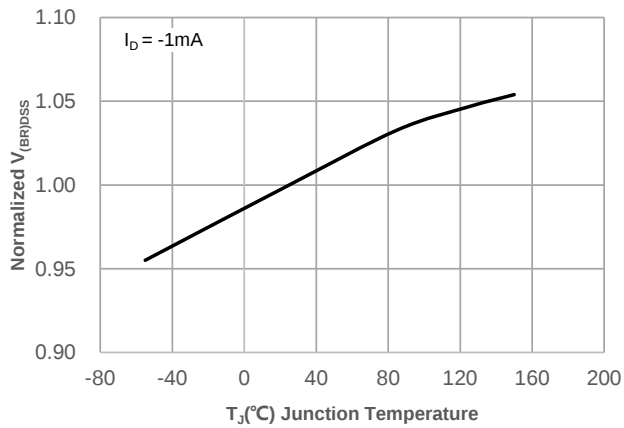


Figure 12: Normalized on Resistance vs. Junction Temperature

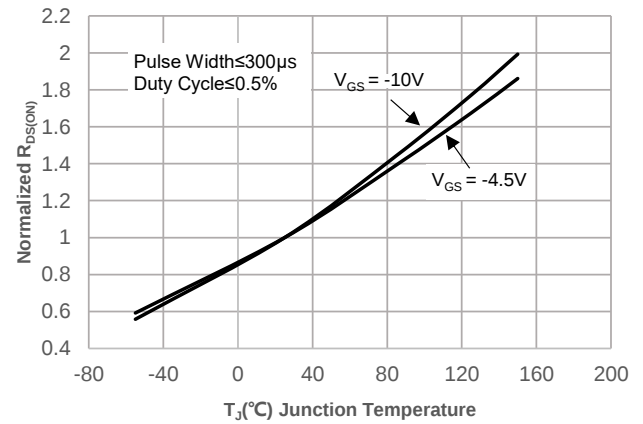


Figure 13: Normalized Threshold Voltage vs. Junction Temperature

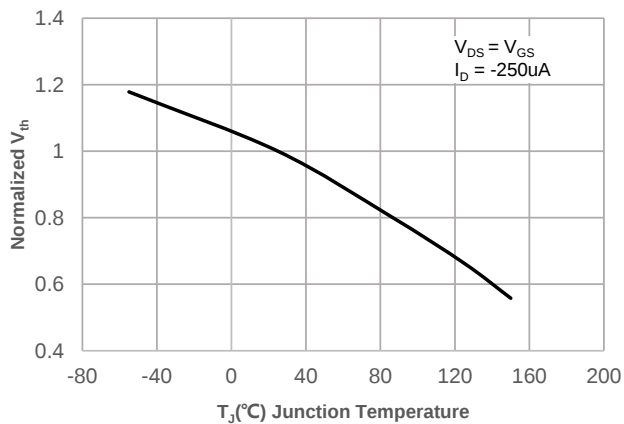


Figure 14: $R_{DS(ON)}$ vs. V_{GS}

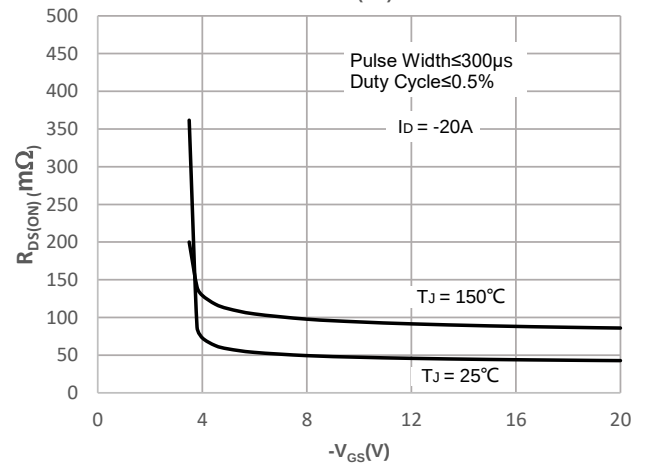
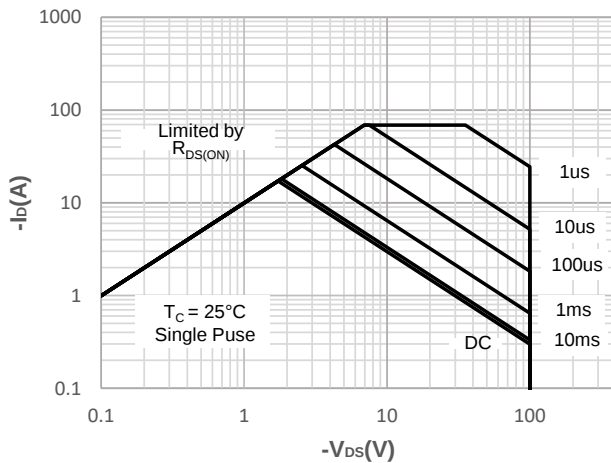


Figure 15: Maximum Safe Operating Area



Test Circuit

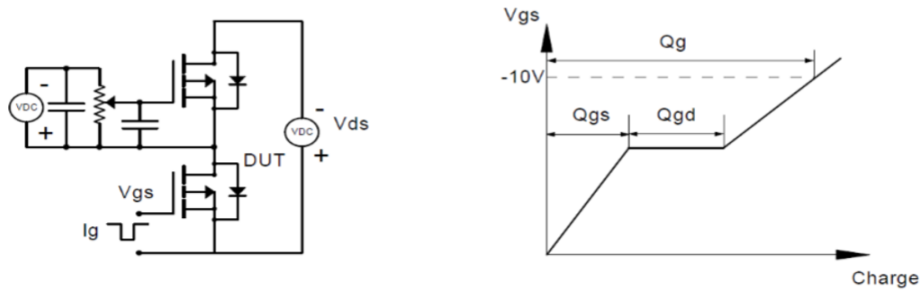


Figure 1: Gate Charge Test Circuit & Waveform

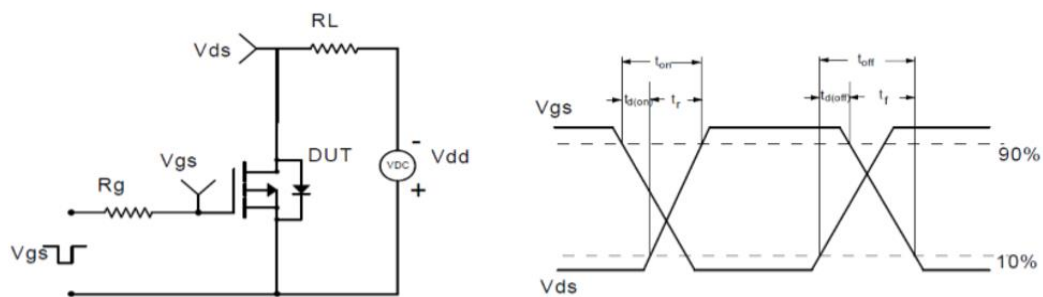


Figure 2: Resistive Switching Test Circuit & Waveform

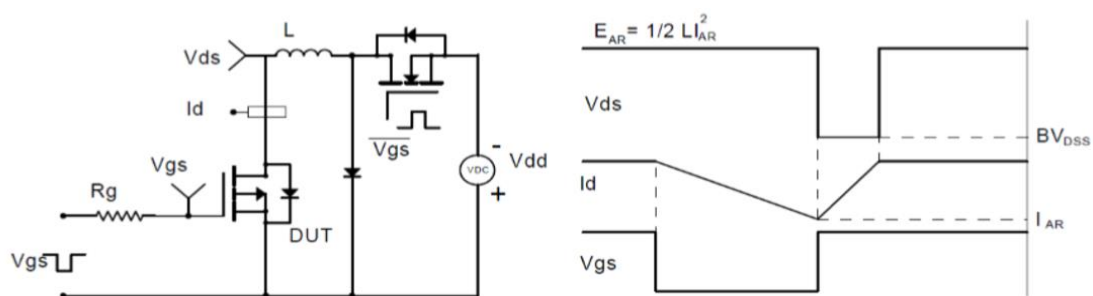


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

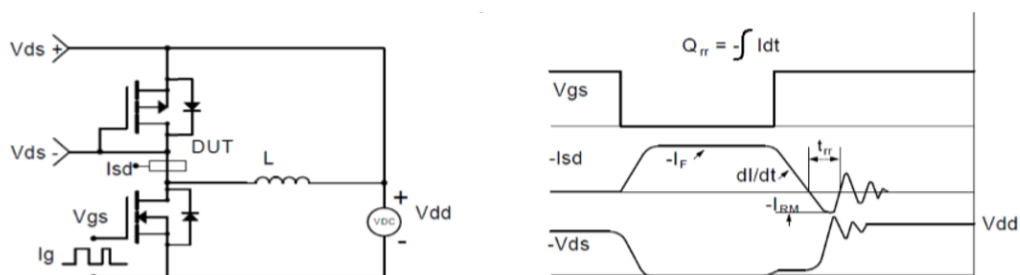
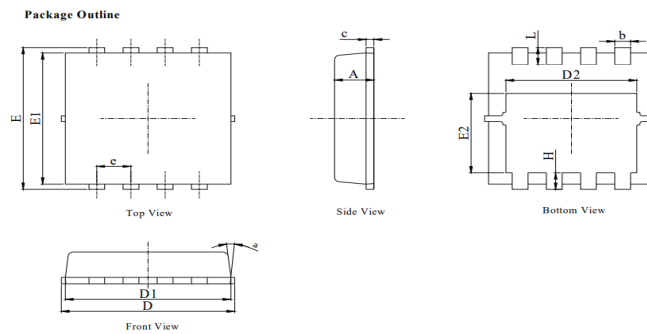


Figure 4: Diode Recovery Test Circuit & Waveform

Package Mechanical Data(PDFN3X3-8L)

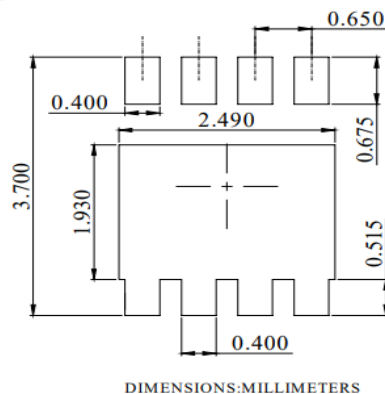


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. ALL DIMENSIONS IN MILLIMETER (ANGLE IN DEGREE).
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM.	MILLIMETER		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.20	0.25
D	3.00	3.15	3.25
D1	2.95	3.05	3.15
D2	2.39	2.49	2.59
E	3.20	3.30	3.40
E1	2.95	3.05	3.15
E2	1.70	1.80	1.90
e	0.65 BSC		
H	0.30	0.40	0.50
L	0.25	0.40	0.50
a	---	---	15°

Recommended Soldering Footprint



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